AMENDMENT TO THE SPECIFICATION

On page 14, please amend the paragraph commencing on line 11 as follows:

Referring to Figure 2, a number of clock domains are illustrated. The various clock domains relate to corresponding components of system 100 of Figure 1. Accordingly, ZB bus domain 201 (ZCLK) corresponds to the clock domain of ZB bus 101 of Figure 1. Likewise, switch domain 210 corresponds to switch 110, BR1 domain 215 corresponds to BR1 115, ~~SCD domain 219 corresponds to SCD unit 119~~ and MC domain 204 corresponds to the MC unit 104 of Figure 1. Furthermore, in reference to the MC domain 204, since four memory channels 0-3 are exemplified in the MC unit 104 of Figure 1, there may be four separate sub-clock domains to handle the data transfer individually. The four domains are noted as domains MCCLK0-MCCLK3 within memory controller clock domain 204. One or more of the clock signals from clock unit 130 may be operably coupled to the various domains shown in Figure 2 to provide clock signals, such as ZCLK and MCCLK0-MCCLK3.

On page 15, please amend the paragraph commencing on line 1 as follows:

In one embodiment, the processors SB-1 operate at a frequency in which the base rate is divided by a fixed divisor of 2. The ZB bus domain operates at a frequency having a divisor fixed at 4 (one-half the CPU clock rate). MC domain 204 in one embodiment may be set having a divisor value from 4 to 32. Switch domain 210 may operate at a frequency having a divisor value from 4 to 15. Other components of Figure 1~~, such as SCD domain 219,~~ may operate having a divisor value from 4 to some integer number. In this particular embodiment, the various modules operate at a clock frequency which is equal to or slower than ZB bus clock domain 201. Accordingly, the data transfer from the ZB bus domain to one of the other domains will be a transfer of data between two domains having the same clock frequency or from a higher clock frequency to a lower clock frequency. Alternatively, data flow from one of the domains 204, 210, 215~~, 219~~ to the ZB bus domain entails data transfer between domains of equal clock frequency or

from a slower clock frequency to a higher clock frequency. It is to be noted that in other embodiments, domains transferring data to the ZB bus may operate at a higher clock frequency than the ZB bus domain. However, for the example system 200 shown in Figure 2, the data transfer to the ZB bus domain from the other clock domains are assumed to be either at the same clock frequency or from a slower clock domain to the higher ZB bus clock domain.